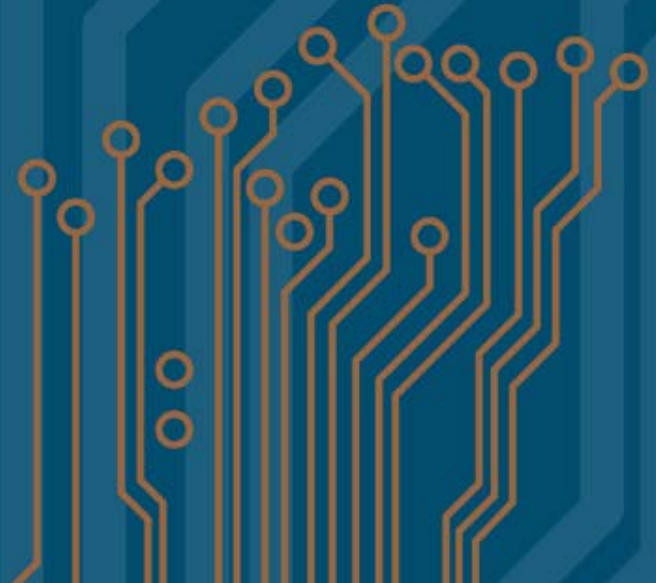




# ***DDi Technology Roadmap***

***2009***



# DDi Technology Roadmap

- **‘DDi Standard’**  
*DDi’s current everyday capability with no premium.*
- **‘DDi Advanced’**  
*DDi’s current everyday capability with a small premium*
- **‘DDi Engineering’** = *DDi has experience with and can fabricate on request with a significant premium.*
- **‘DDi Development’** = *Process development in-process based on customer demand.*

# DDi Technology Roadmap

		Standard	Advanced	Engineering	Development
<b>Trace &amp; Space</b>	External Trace	0.004"	0.003"	0.0025"	0.002"
	External Space	0.004"	0.003"	0.0025"	0.002"
	Internal Trace	0.004"	0.003"	0.0025"	0.002"
	Internal Space	0.004"	0.003"	0.0025"	0.002"
<b>Drilled Via Size</b>	Drill Diameter	0.010"	0.008"	0.006"	0.004"
	Pad Diameter	0.020"	0.016"	0.012"	0.004"
<b>Aspect Ratio</b>	0.006" drill		6.5:1	10:1	14:1
	0.008" drill	8:1	10:1	12:1	16:1
	0.010" drill	10:1	12:1	16:1	18:1
	0.012" drill	10:1	14:1	18:1	20:1
	0.0135" drill	10:1	16:1	20:1	24:1
<b>Microvia</b>	Via Diameter	0.006" & 0.005"	0.004"	0.006"	0.004"
	Pad Diameter	0.012" & 0.010"	0.008"	0.010"	0.007"
	Aspect Ratio	0.6:1	0.8:1	1:1	1:1
		2009	2009	2009	2010 2009



# DDi Technology Roadmap

		Standard	Advanced	Engineering	Development
<b>Microvia Stack-up</b>	# Microvia layers	1+1	2+2 3+3 4+4	6+6	>7+7
	Buried Sub	Yes	Yes	Yes	Yes
	Stacked MicroVias	No	Yes	Yes	Yes
<b>Microvia Materials</b>	→	Std FR4 Laser Prepregs	Low loss Epoxy Polyimide & BT	Microwave	Film Lased BUM
<b>Attributes</b>	Layer Count	Up to 24	26 to 44	46 to 60	>60
	Thickness	Up to 0.130"	Up to 0.300"	Up to 0.400"	>0.400"
<b>Laminate Materials</b>	→	High Temp FR4 Lead Free Assembly HDI Flex & Rigid Flex	High Speed Low Loss BT & Polyimide Stablcor	PTFE RF & Microwave	LCP Film Based Non-Reinforced
		2009	2009	2009	2010 2009



# DDi Technology Roadmap

		Standard	Advanced	Engineering	Development
Embedded Passives		Buried Capacitance BC2000™	Buried Resistors FaradFlex™ Dupont™ HK-04	High Dk Ceramic Filled	Embedded Active/Passive Devices
	→				
Surface Finishes		HASL OSP Immersion Tin	Lead free HASL Immersion Silver Immersion Gold	E-Less Gold Multiple	ENEPIG Neutral Eless Au Ormecon
	→				
Solder Mask	Registration	+/-0.0025"	+/-0.002"	+/-0.001"	<0.001"
	Min opening	0.008"	0.006"	0.005"	0.004"
Via Fill/Cap Plate	Min Drilled hole	0.012"	0.010"	0.008"	0.008"
	Aspect ratio	8:1	10:1	6.5:1	10:1
		Non-CVF & CVF	Non-CVF & CVF	Non-CVF	Copper CVF
		2009	2009	2009	2010 2009



# DDi Technology Roadmap

## Current Process Highlights

- **Laser Direct Imaging for Improved Feature Size Capability & Registration**
- **Reverse Pulse Plating System, Current capability up to 20:1 aspect ratio**
- ***FLAT-WRAP™* Technology (wrap plating solution)**
- **Process Verification and Capability Studies of High Aspect Ratio Interconnect Reliability with IST**
- **High Yield Fine Line Etching, (Cupric Chloride Etching)  
Ultra thin Copper Foils**
- **Enhanced Registration of Higher Layer Count Boards With the use of Vision Based Post Etch Punch**
- **Via in Pad (Laser Drilled Microvias with Solid Copper Plate)**
- **Stacked MicroVias (SMV™) - UV, UV/C02 & C02 Laser drill systems (13)**
- **Comprehensive Process Analysis Lab**
- **Controlled Impedance Tolerance to  $\pm 5\%$**
- **Flying Probe TDR Testing (Internal & panel)**



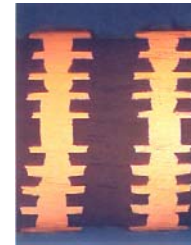
# DDi Technology Roadmap

## Planned Process Improvements

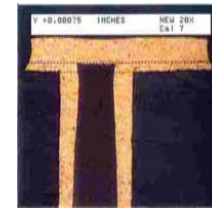
- Increase Plating Aspect Ratio to >20:1
- Reduce Controlled Impedance Tolerance to  $\leq \pm 5\%$
- Introduction of Advanced Photo-Resists
- Advanced photo-tool registration systems
- Continual Addition of New Advanced Materials
- Continuous evaluation of New Materials for Lead Free Assembly  
(245°C - 288° C)

# DDi Enabling Technology

- Laser Drilling Microvia Technology
- Laser Direct Imaging for HDI
- Stacked MicroVias (SMV™) – Solid Copper Plate
- Reverse Pulse Plating – High Aspect Ratio
- *FLAT-WRAP™* Technology (wrap plating solution)
- Flying Probe TDR for Impedance Testing
- Embedded Passives (Capacitance & Resistance)
- Green Materials (Halogen & Lead Free)
- Hybrid Material Construction (PTFE & FR4)
- Thermal Management – Copper Core/STABLCOR®
- NextGen Technology (3G-SMV™, HDI-Link™, Sub-Link™)
- Solid Copper Via (ThermalVia™)
- Deep Blind Vias (DpBV™)
- Deep Microvias (DpMV™)
- Deep Stacked Microvias (DpSMV™)
- Embedded Heater Circuits (EHC™)



UV/CO2 laser



Robotic TDR



Orbotech LDI  
Paragon 8800



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